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SPECIFICATION

MULTIPLE STORAGE NODE ACTIVE PIXEL SENSORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to active pixel sensors and active pixel sensor arrays. More particularly, the present invention relates to active pixel sensors having multiple storage nodes, and applications, such as still cameras, that employ an array of active pixel sensors having multiple storage nodes.

2. The Background Art

In still-camera applications with randomly-addressable CMOS active pixel sensors, the problem of how to implement a short-exposure interval with a long read out interval exists. A typical active pixel area-array image sensor is disclosed in Hurwitz et al., "An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras", SPIE Vol. 3019, pp 115-124 and comprises a plurality of rows and columns of pixel sensors. The most common method of exposure for this type of sensor array is to cyclicly scroll through the rows so that the integration duration for each row is the same, but can be shorter than the total readout interval. This method of exposure control is known as an electronic shutter.

There are two problems with this type of electronic shutter. First, since each row scans a different time interval, there will be motion artifacts (the shape of moving objects

will be distorted). Second, this scheme requires a very high conversion rate analog-to-digital converter (ADC) implementation. For example, if the array has 1 million pixels, and the read out duration is 1/100 sec (about the maximum acceptable for a hand-held camera), the required conversion rate is 100 million samples/sec. Since the state of the art for commercial ADCs with the required accuracy (10 bits) is about 20 million samples/sec, this means that a total of 5 ADCs would have to be used to allow for 1/100 sec exposures.

To overcome some of the problems associated with the electronic shutter, various schemes have been proposed in the prior art. One such scheme is disclosed in Serial No. 08/969,383, entitled "Intra-Pixel Frame Storage Element, Array and Electronic Shutter Method Suitable for Electronic Still Camera Applications", filed November 13, 1997, and expressly incorporated herein by reference. Despite the improvement in the electronic shutter identified by the above recited scheme, it nonetheless takes a significant amount of time to read out an image. As a consequence of these continuing problems, the capture of multiple images from the imager in rapid succession is difficult because the time period is too brief.

Another problem readily appreciated by those of ordinary skill in the art when a comparison of the output of a digital still camera is made with the image quality produced by a film camera is that an improvement in dynamic range compression must be made. Currently, the limitations on dynamic range capability result in burn-out of highlights and, as such, the critical exposure values in a digital imager compare poorly to

the quality to those of film. It is typically understood that to improve the image quality in a photograph, a compression scheme should increase the useful dynamic range in the imager by at least ten times. This is critically true for the highlights in the image. For the dynamic range compression schemes presently available in the art employing non-linear charge to voltage conversion in the pixel, a satisfactory dynamic range compression has not yet been achieved.

A still camera having the capability of capturing multiple images in rapid succession would help to secure numerous benefits not provided for by the prior art. First, multiple images with different focus settings may be used to reconstruct an image that is sharp. Second, multiple images with different exposure settings or sensitivities may be used to reconstruct an image with wide dynamic range. Third, multiple images can be captured with a known time interval between them for the purpose of measuring velocity of objects captured within the images. Fourth, images stored in rapid succession can be used for temporal bracketing, including capturing images from the recent past before the "shutter release" button is pressed. Fifth, images may be taken immediately before and after firing an electronic flash in order to capture differently-lighted images. The flash-exposed image and the image exposed in natural light may then be combined. Sixth, multiple images may be captured through separate color filters (e.g., red, green and blue filters) to capture a color image.

It is therefore an object of the present invention to provide an active pixel sensor having multiple storage nodes for capturing multiple images.

It is a further object of the present invention to provide an array of active pixel sensors having multiple storage nodes for capturing multiple images.

BRIEF DESCRIPTION OF THE INVENTION

According to the present invention, active pixel sensors having multiple storage nodes suitable for use in an array of storage pixel sensors is disclosed. The array may be used in still camera applications to capture multiple images in rapid succession. The captured images may then be manipulated to construct a new image or for other purposes, such as measuring the velocity of objects within the captured images.

In a first embodiment of the present invention, the active pixel sensor includes a plurality of storage nodes, one row select line for selecting the plurality of storage nodes, and a plurality of column output lines upon which the images stored in the plurality of storage nodes may be read out. Column circuits may be employed to perform a function on the images stored on the plurality of storage nodes.

In a second embodiment of the present invention, the active pixel sensor includes a plurality of storage nodes, a plurality of row select lines connected to the plurality of storage nodes and a single column output line upon which the images stored in the plurality of storage nodes may be read out. One or more row decoding circuits may be connected to the row select lines to select a row of one of the stored images within the storage nodes.

In a third and fourth alternative embodiments of the present invention one of which provides a current-mode output, the active pixel sensor includes a plurality of storage nodes, a plurality of image select signals for selecting the plurality of storage nodes, and a single row select line for placing selected images on a column output line. The use of the image select signals in combination with the row select transistor eliminates the need for the multiple row select signals of the third embodiment.

In a fifth embodiment of the present invention, the storage pixel sensor includes multiple storage nodes, multiple row select lines, and multiple column output lines.

In a sixth embodiment of the present invention, the active pixel sensor includes two storage nodes connected to a differential amplifier controlled by a single row select line to provide differential current output. Column circuits may be used to directly sense a difference between the two images stored on the two storage nodes. The differential read out circuit may be used for various purposes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an imager suitable for use with the embodiments of active pixel sensors according to the present invention

FIG. 2 is a schematic diagram of an N-channel MOS implementation of a known active pixel sensor circuit having a single storage node.

FIG. 3 is a timing diagram illustrating the operation of the active pixel sensor depicted in FIG. 2.

FIG. 4 is a diagram of a photosensor suitable for use according to the present invention.

FIGS. 5, 6, 7, 8, 9 and 10 are schematic diagrams of active pixel sensors having multiple storage nodes according to first through six embodiments of the present invention.

FIGS. 11A and 11B are alternative timing diagrams for the operation of the active pixel sensors according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

FIG. 1 is a block diagram of an active pixel imager 10 suitable for use according to the present invention. In the imager 10, the active pixel sensors are arranged in rows and columns in a pixel sensor array 12. To extract the analog pixel information from the pixel sensor array 12 for processing by an analog-to-digital converter (ADC) 14, a row decoder circuit 16, a column sampling circuit 18, and a counter 20 are employed. The

row decoder 14 selects rows from the pixel sensor array 12 in response to a row enable signal 22 and signals from the counter 20. The column sampling circuit 18 is also driven from the counter 20 and further includes a multiplexer that couples the sampled columns as desired to the ADC in response to signals from counter 20.

In a typical implementation, the higher-order bits from counter 20 are used to drive the row decoder circuit 14 and the lower-order bits are used to drive column sampling circuit 20 to permit extraction of all pixel information from a row in the pixel sensor array 12 prior to selection of the next row by row decoder circuit 14. Row decoders, column sampling circuits, and counters suitable for use in the imager 10 are well known to those of ordinary skill in the art, and will not be described herein in detail to avoid overcomplicating the disclosure and thereby obscuring the present invention.

Referring now to FIG. 2, a schematic diagram of a known active pixel sensor 30 with a single embedded storage element is shown. The active pixel sensor 30 is implemented with N-channel MOS transistors. Those of ordinary skill in the art will appreciate that the active pixel sensor 30 may otherwise be implemented with all P-channel MOS transistors or a combination of P-channel and N-channel MOS transistors. In active pixel sensor 30, a photodiode 32 has an anode connected to ground and a cathode connected to the source of N-Channel MOS reset transistor 34. The drain of N-Channel MOS reset transistor 34 is connected to Vref and the gate of N-Channel MOS reset transistor 34 is connected to the global RESET line indicated by reference numeral 24 in FIG. 1. The RESET line is preferably driven to a voltage at least a threshold above

Vref to set the cathode of the photodiode 32 to Vref.

The cathode of photodiode 32 is also connected to a first source/drain of N-channel MOS transfer transistor 36. A second source/drain of N-Channel MOS transfer transistor 36 is connected to a first terminal of a storage element 38 and also to the gate of N-channel MOS readout transistor 40. A second terminal of the storage element 38 is connected to reference potential shown as ground. The gate of N-Channel MOS transfer transistor 36 is connected to the global XFR line indicated by reference numeral 26 in FIG. 1. The connection of the second source/drain of N-Channel MOS transfer transistor 36 to the first terminal of storage element 38 and also to the gate of N-Channel MOS transistor 40 forms a storage node 42. The drain of N-channel MOS readout transistor 40 is connected to Vcc, and the source of N-channel MOS readout transistor 40 is connected to the drain of N-channel MOS row select transistor 44. The gate of N-channel MOS row select transistor 44 is connected to a ROW SELECT line, one of which is depicted by reference numeral 28 in FIG. 1, and the source of N-channel MOS row select transistor 44 is connected to a column output line.

It should be appreciated that associated with the storage node 42 are the N-channel MOS transfer transistor 36 to isolate the storage node 42 from further collection of photocharge by the cathode of photodiode 32 when an integration period to be described below has ended, the N-channel MOS readout transistor 40 to sense the charge accumulated at storage node 42, and the storage element 38 to store charge. Further, as disclosed in co-pending application serial number 09/099,116, entitled

"ACTIVE PIXEL SENSOR WITH BOOTSTRAP AMPLIFICATION", by Richard B. Merrill and Richard F. Lyon, filed on June 17, 1998, having attorney docket no. FOV-013, and assigned to the same assignee as the present invention, and expressly incorporated herein by reference, the storage element 38 may be omitted and charge stored on the gate of N-channel MOS readout transistor 40 or that other capacitive means of charge storage may be employed.

To better understand the operation of the active pixel sensor 30, FIG. 3 illustrates a timing diagram of the RESET, XFR and ROW SELECT signals depicted in FIG. 2. The active pixel 30 is reset by turning on both N-channel MOS reset transistor 34 and N-channel MOS transfer transistor 36 as shown by the HIGH level of both the RESET and XFR signals at 50 and 52. Then the N-channel MOS reset transistor 34 is turned off at the falling edge 54 of RESET 50 so that integration of photocurrent from photodiode 32 can begin. The photocurrent integration period is indicated by reference numeral 56.

While N-channel MOS transfer transistor 36 is turned on, the capacitance of the storage element 38 adds to the capacitance of the photodiode 32 during integration, thereby increasing the charge capacity and the range of the active pixel sensor 30. This also reduces variation in the pixel output due to capacitance fluctuations since gate oxide capacitance from which storage element 38 is formed is better controlled than junction capacitance of the photodiode 32.

When the integration is complete (determined by external exposure control), the

N-channel MOS transfer transistor 36 turns off at falling edge 58 of XFR to isolate the voltage level corresponding to the integrated photocharge onto the storage element 38. Shortly thereafter, the photodiode 32 itself is preferably reset to the reference voltage by again turning on N-channel MOS reset transistor 34 as indicated by rising edge 60 of RESET. This action will prevent the photodiode 32 from continuing to integrate during the read out process and possibly overflowing excess charge into the substrate which could effect the integrity of the signal on the storage element 38.

After the N-channel MOS transfer transistor 36 is turned off, the read out process can begin. Each of the active pixel sensors in a row is read when a ROW SELECT signal pulse as shown in FIG. 3 is applied to the gate of the N-channel MOS row select transistor 44 in an active pixel sensor 30. In the operation of active pixel sensor 30, a voltage related to the voltage found on storage node 42 is sensed by N-Channel MOS readout transistor 40 and placed on the column output line when N-channel row select transistor 44 is turned on. The XFR signal stays low until all of the rows have been read out or another cycle is initiated.

A photodiode suitable for use according to the present invention is disclosed in co-pending application serial No. _____, entitled "COLOR SEPARATION IN AN ACTIVE PIXEL CELL IMAGING ARRAY USING A TRIPLE-WELL STRUCTURE", by Richard B. Merrill, filed on xx, having attorney docket no. FOVE-3300, and assigned to the same assignee as the present invention, and expressly incorporated herein by reference. The photodiode disclosed therein has a triple-well structure that provides

three overlapping photodetectors in the photodiode. In the embodiments of the active pixel sensors of the present invention to be disclosed below, each of these overlapping photodetectors may be connected to a different one of the multiple storage nodes in the active pixel sensors.

Another photosensor 70, suitable for use according to the present invention is illustrated in FIG. 4. Photosensor 70 includes first and second photodiodes 72 and 74. First and second photodiodes 72 and 74 are arranged in an annular manner, such that first photodiode 72 provides a low sensitivity area in comparison to the high sensitivity area of the larger second photodiode 74. Because the first and second photodiodes 72 and 74 have the same geometric center, they will sample the same average incident photon flux of the image when the spacial signal variation is linear. A dynamic range compression advantage provided by the photosensor 70 is that first and second photodiodes 72 and 74 will sample the photo current during the same time interval. It will be readily appreciated by those of ordinary skill in the art that this property could be very useful, for example, in flash exposures.

In the photosensor 70, each of the first and second photodiodes 72 and 74 will generate photo current in proportion to its area. With recent advances in process technologies, the active area openings and the photo diodes can be made small enough to provide a photo current ratio that is quite large, on the order, for example, of about 50:1 for a 6 micron x 6 micron pixel. It is presently contemplated that each of the photodiodes 72 and 74 in the photosensor 70 may be connected to a separate one of

the multiple storage nodes to be described below.

According to the present invention, the active pixel sensors in an imager 10 such as that illustrated in FIG. 1 may include multiple storage nodes so that an array of pixel sensors each having multiple storage nodes may be used to capture more than a single image. Several embodiments of a storage pixel sensor having multiple storage nodes are described below. The embodiments of storage pixel sensors described below are implemented with N-channel MOS transistors. Those of ordinary skill in the art will appreciate that the storage pixel sensors below may otherwise be implemented with P-channel MOS transistors or a combination of N-channel and P-channel MOS transistors.

Referring now to FIGS. 5–10, schematic diagrams of six embodiments of active pixel sensors having multiple storage nodes according to the present invention are shown. In each of the embodiments of the pixel sensors 100-1 through 100-6 depicted in FIGS. 5–10, the storage pixel sensor 100 includes a photodiode 102 having an anode connected to ground and a cathode connected to the source of an N-channel MOS reset transistor 104. The gate and drain of N-channel MOS reset transistor 104 are connected to a RESET signal and to Vref, respectively.

Further, FIGS. 5–9 each include a plurality of storage nodes 106-1 through 106-n. A first storage node 106-1 connects the first terminal of a storage element 108-1, a first source/drain of N-channel MOS transfer transistor 110-1, and the gate of N-channel MOS readout transistor 112-1. A nth storage node 106-n connects the first terminal of a

storage element 108-n, a first source/drain of N-channel MOS transfer transistor 110-n, and the gate of N-channel MOS readout transistor 112-n. The cathode of the photodiode 102 is also connected to a second source/drain of N-channel MOS transfer transistors 110-1 and 110-n. The gates of N-channel MOS transfer transistors 110-1 and 110-n are connected XFR1 and XFRn signals, respectively. The storage elements 108-1 and 108-n each have a second terminal connected to a fixed potential shown as ground.

In the embodiment of active pixel sensor 100-5 depicted in FIG. 9, additional storage nodes 106-n/i and 106-(n-j), are depicted to demonstrate that the multiple storage nodes may be matrixed between ROW SELECT1 through ROW SELECT i and column output lines 1 through j. Storage node 106-n/i connects the first terminal of a storage element 108-n/i, a first source/drain of N-channel MOS transfer transistor 110-n/i, and the gate of N-channel MOS readout transistor 112-n/i. Storage node 106-(n-j) connects the first terminal of a storage element 108-(n-j), a first source/drain of N-channel MOS transfer transistor 110-(n-j), and the gate of N-channel MOS readout transistor 112-(n-j). The cathode of the photodiode 102 is also connected to a second source/drain of N-channel MOS transfer transistors 110-n/i and 110-(n-j). The gates of N-channel MOS transfer transistors 110-n/i and 110-(n-j) are connected XFRn/i and XFR(n-j) signals, respectively. The storage elements 108-n/i and 108-(n-j) each have a second terminal connected to a fixed potential shown as ground.

In FIG. 10, because a differential read out circuit is placed in the active pixel element 100-6, only two storage nodes 106-1 and 106-2 are depicted. The first storage

node 106-1 connects the first terminal of a storage element 108-1, a first source/drain of N-channel MOS transfer transistor 110-1, and the gate of N-channel MOS readout transistor 112-1. The second storage node 106-2 connects the first terminal of a storage element 108-2, a first source/drain of N-channel MOS transfer transistor 110-2, and the gate of N-channel MOS readout transistor 112-2. The cathode of the photodiode 102 is also connected to a second source/drain of N-channel MOS transfer transistors 110-1 and 110-2. The gates of N-channel MOS transfer transistors 110-1 and 110-2 are connected XFR1 and XFRn signals, respectively. The storage elements 108-1 and 108-2 each have a second terminal connected to a fixed potential shown as ground.

In the operation of the active pixel sensors 110-1 through 110-6, the active pixel sensors are reset and charge is accumulated in a manner similar to that described above with respect to FIG. 2. However, it should be appreciated that the operation may be performed differently than described above with reference to FIG. 2, in that the integration periods for the images stored on each of the storage nodes may be made different by applying the XFR1 through XFRn signals to the gates of N-channels MOS transfer transistors 110-1 and 110-n, respectively, for different durations or at different times. For such an implementation, instead of the single global XFR line as depicted in FIG. 1 there will be XFR1 through XFRn global transfer lines. In FIGS. 11A and 11B, alternative timing diagrams of the RESET, XFR1 and XFRn signals for the active pixel sensors according to the present invention are depicted. Nonetheless, a single global XFR line may still be employed. This is particularly advantageous, for example, when the photosensor being employed in the active pixel sensor is the annular photosensor 70

depicted in FIG. 4.

In FIG. 11A, with XFR1 signal HIGH, the RESET signal makes a transition at falling edge 150 to begin the accumulation of charge on storage node 106-1. When XFR1 signal makes a transition at falling edge 152, the accumulation of charge on storage node 106-1 stops. The RESET signal is then makes a transition at rising edge 154 to reset the voltage at the cathode of the photodiode 102. The XFRn signal then makes a transition at rising edge 156. When the RESET signal makes a transition at falling edge 158, accumulation of charge on storage node 106-n begins. When the XFRn signal makes a transition at falling edge 160, the accumulation of charge on storage node 106-n stops.

In FIG. 11B, with XFR1 and XFRn signals HIGH, the RESET signal makes a transition at falling edge 170 to begin the accumulation of charge on storage nodes 106-1 and 106-2. When XFR1 signal makes a transition at falling edge 172, the accumulation of charge on storage node 106-1 stops, and the accumulation of charge on storage node 106-n continues until the XFRn signal makes a transition at falling edge 174.

In the embodiment of active pixel sensor 100-1 depicted in FIG. 5, voltages present on storage nodes 106-1 through 106-n are read out onto separate column output lines 116-1 through 116-n, respectively, by the same row select signal. Accordingly, the drain of each N-channel MOS readout transistor 112-1 through 112-n is connected to Vcc, and the source of each N-channel MOS readout transistor 112-1 through 112-n is

connected to the drain of an N-channel MOS row select transistor 114-1 through 114-n, respectively. The gates of N-channel MOS row select transistors 114-1 through 114-2 are each connected to the same ROW SELECT signal, and the source of N-channel MOS row select transistor 114-1 through 114-2 are connected to the column output lines 116-1 through 116-n, respectively.

In the operation of the active pixel sensor 100-1, during the reading out of the images on the first and second column output lines, column circuits (not shown) connected to the column output lines 116-1 through 116-n, respectively, may be used to select a stored image provided on the storage nodes 106-1 through 106-n. Further, column circuits may be used to perform some function on both stored images, such as performing the a linear combination of the two images.

In the embodiment of active pixel sensor 100-2 depicted in FIG. 6, voltages present on storage nodes 106-1 through 106-n are read out separately onto the same column output line 118, by ROW SELECT1 through ROW SELECTn signals. Accordingly, the drain of each N-channel MOS readout transistor 112-1 through 112-n is connected to Vcc, and the source of each N-channel MOS readout transistor 112-1 through 112-n is connected to the drain of N-channel MOS row select transistors 120-1 through 120-n, respectively. The gates of N-channel MOS row select transistors 120-1 through 120-n are each connected to ROW SELECT1 through ROW SELECTn signals, respectively, and the sources of N-channel MOS row select transistors 120-1 through 120-n are connected to the single column output line 118.

In the operation of active pixel sensor 100-2, the image stored on storage node 106-1 will be read out in response to a HIGH ROW SELECT1 signal , and the image stored on storage node 106-n will be read out in response to a HIGH ROW SELECTn signal. It should be understood that the imager 10 depicted in FIG. 1 will further include additional decoding circuits for providing the ROW SELECT1 through ROW SELECTn signals.

In the embodiment of active pixel sensor 100-3 depicted in FIG. 7, voltages present on storage nodes 106-1 through 106-n are read out separately onto a single column output line 122 in response to IMAGE SELECT1 through IMAGE SELECTn signals, applied to N-channel MOS image select transistors 124-1 through 124-n, respectively, and a ROW SELECT signal. Accordingly, the drains of N-channel MOS readout transistors 112-1 through 112-n are each connected to Vcc, and the sources of N-channel MOS readout transistors 112-1 through 112-n are connected to the drains of N-channel MOS image select transistors 124-1 through 124-n, respectively. The gates of N-channel MOS image select transistors 124-1 through 130-n are connected to IMAGE SELECT1 through IMAGE SELECTn signals, respectively. The sources of N-channel MOS image select transistors 124-1 through 124-n are connected to the drain of N-channel MOS row select transistors 126. The gate of N-channel MOS row select transistor 126 is connected to a ROW SELECT signal, and the source of N-channel MOS row select transistor 126 is connected to a column output line 122.

In the operation of active pixel sensor 100-3, the image stored on storage node 106-1 will be read out in response to a HIGH ROW SELECT signal and a HIGH IMAGE SELECT1 signal , and the image stored on storage node 106-n will be read out in response to a HIGH ROW SELECT signal and a HIGH IMAGE SELECTn signal. It should be understood that the imager 10 depicted in FIG. 1 will further include global IMAGE SELECT1 through IMAGE SELECTn lines. The use of the global IMAGE SELECT1 through IMAGE SELECTn signals in combination with the ROW SELECT signal eliminates the need for the additional row decoding required in the second embodiment.

In the embodiment of active pixel sensor 100-4 depicted in FIG. 8, voltages present on storage nodes 106-1 through 106-n are read out in a current mode onto a single column output line 128 in response to IMAGE SELECT1 through IMAGE SELECTn signals, respectively, and a ROW SELECT signal. Accordingly, the drains of N-channel MOS readout transistors 112-1 through 112-n are connected together, and to the source of an N-channel MOS row select transistor 130. The sources of N-channel MOS readout transistors 112-1 through 112-n are connected to IMAGE SELECT1 through IMAGE SELECTn signals, respectively. The gate of N-channel MOS row select transistor 130 is connected to a ROW SELECT signal, and the drain of N-channel MOS row select transistor 130 is connected to a column output line 128.

In the operation of active pixel sensor 100-4, the column output line 128 is connected to the drain of the N-channel MOS row select transistor 130. To place

current representing the stored image on the column output line 128, the image stored at storage node 106-1 will be selected by a LOW IMAGE SELECT1 signal, and the image stored at storage node 106-n will be selected by a LOW IMAGE SELECTn signal. The current-mode output on column output line 128 is therefore controlled by the IMAGE SELECT1 through IMAGE SELECTn signals. The column output line 128 output must be kept biased to a high enough voltage that the non-selected N-channel MOS readout transistors 112-1 through 112-2 do not start conducting backward. Further, it should be appreciated that the voltage drivers for the IMAGE Select1 through IMAGE SELECTn signals must be capable of sinking all the column current from the selected row.

In the embodiment of active pixel sensor 100-5 depicted in FIG. 9, the voltages present on storage nodes 106-1 through 106-n/i are read out onto column output lines 132-1 through 132-j, respectively, by the ROW SELECT1 signal, and the voltages present on storage nodes 106-(n-j) through 106-n are read out onto column output lines 138-1 through 132-j, respectively, by the ROW SELECT i signal. Accordingly, the drain of each N-channel MOS readout transistors 112-1 through 112-n are connected to Vcc, and the source of each N-channel MOS readout transistor 112-1 through 112-n is connected to the drain of an N-channel MOS row select transistor 134-1 through 134-n, respectively. The gates of N-channel MOS row select transistors 134-1 through 134-n/i are each connected to the ROW SELECT1 signal, and the gates of N-channel MOS row select transistors 134-(n-j) through 134-n are each connected to the ROW SELECT i signal. The sources of N-channel MOS row select transistors 134-1 through 134-(n-j) are connected to first column output line 132-1, and the sources of N-channel MOS row

select transistors 134-n/i through 134-j are connected to the column output line 132-j.

In the operation of the active pixel sensor 110-5, charge stored on any of the storage nodes 106-1 through 106-n in is read out in response to the application of the ROW SELECT1 through ROW SELECT i signals applied to the gate of N-channels MOS row select transistors 134-1 through 134-n to which the storage node 106-1 through 106-n is coupled and by sensing the column output line 132-1 through 132-j to which the storage node 106-1 through 106-n is coupled. For example to select a stored image provided on the storage nodes 106-1, the ROW SELECT1 signal will be asserted and the COLUMN OUTPUT1 line 138-1 will be chosen. As such when numerous storage nodes are employed, the matrixing of the storage nodes 106-1 through 106-n between several ROW SELECT lines and several column output lines reduces the number of additional row and column lines required. It should also be understood that instead of the single global XFR line depicted in FIG. 1 that there will be XFR1 through XFRn global transfer lines.

In the embodiment of active pixel sensor 100-6 depicted in FIG. 10, voltages present on storage nodes 106-1 and 106-2 are read out as a differential signal on column output lines 140-1 and 140-2, by the same row select signal. Accordingly, the N-channel MOS row select transistor 136 and N-channel MOS readout transistors 112-1 and 112-2 are configured as a differential amplifier, such that the source of each N-channel MOS readout transistor 112-1 and 112-2 is connected to the drain of N-channel MOS row select transistor 136, the drains of N-channel MOS readout transistor 112-1 and 112-2 are

connected to first and second column output lines 140-1 and 140-2, respectively, the source of N-channel MOS row select transistor 136 is connected to a column bias line 138, and the gate of N-channel MOS row select transistor 136 is connected to a ROW SELECT signal.

In the operation of active pixel sensor 100-6, the N-channel MOS read out transistors 112-1 and 112-2 and N-channel MOS row select transistor 136 form a differential amplifier, so that when ROW SELECT signal goes HIGH, the N-channel MOS row select transistor 136 is turned on, and the differential signal on storage nodes 106-1 and 106-2 is read out on column outputs 140-1 and 140-2. The differential read out of the storage nodes 106-1 and 106-2 may be used in a variety of ways. For example, the differential read out may be used to read out a difference relative to a dark frame. In this manner, correlated noises may be removed, leaving only uncorrelated pixel noises. The differential read out may be also used as a processor for detecting image changes. This change detection is particularly useful in apparatus such as security cameras, as well as for use in automatic object detection for "blue screening". It should be appreciated that the differential read out circuit placed in the active pixel sensor according to this embodiment could also be placed in a column circuit. Placing the differential read out circuit in the column circuit would permit frames to be read out before and after a detected change.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications

than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.